

BUS CYCLE #	BUS DATA [8:0]		
	BUS ctl	DATA	
0	START	OP[0]	ADDRESS [9:2]
1	OP[1]	OP[3]	ADDRESS [17:10]
2	C/D		ADDRESS [26:18]
3	OP[2]		ADDRESS [35:27]
4	C/D	MASTER [3:2]	COUNT [6,4,2]
5	RSRV	MASTER [1:0]	COUNT [7,5,3] COUNT [1:0] ADDRESS [1:0]

FIGURE 4

**One Byte Transfer (MasterCount[7:0] = 00000000)**

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
00000000	00	00	0001	1111	0001
00000000	01	01	0011	1110	0010
00000000	10	10	0111	1100	0100
00000000	11	11	1111	1000	1000

**FIGURE 7a****Two Byte Transfer (MasterCount[7:0] = 00000001)**

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
00000000	01	00	0011	1111	0011
00000000	10	01	0111	1110	0110
00000000	11	10	1111	1100	1100
00000001	00	11	0001	1000	not used - two QB's

**FIGURE 7b**

Four Byte Transfer (MasterCount[7:0] = 00000011)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
00000000	11	00	1111	1111	1111
00000001	00	01	0001	1110	not used - two QB's
00000001	01	10	0011	1100	not used - two QB's
00000001	10	11	0111	1000	not used - two QB's

FIGURE 7C

Eight Byte Transfer (MasterCount[7:0] = 00000111)

Count[7:2]	Count[1:0]	Adr[1:0]	Mask[7:4]	Mask[3:0]	Mask[7:4] and Mask[3:0]
00000001	11	00	1111	1111	not used - two QB's
00000010	00	01	0001	1110	not used - three QB's
00000010	01	10	0011	1100	not used - three QB's
00000010	10	11	0111	1000	not used - three QB'

FIGURE 7d